

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
1875.3760001APPLICATION NO.
To be assignedFIRST NAMED INVENTOR
Minsheng WangFILING DATE
February 25, 2004ART UNIT
2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
PIP	AA1	6,583,742	06-2003	Hossack, David MacDonald	341	144	
	AB1	6,292,124	09-2001	Hanada et al.	341	144	
	AC1	6,124,813	09-2000	Robertson et al.	341	155	
	AD1	6,518,899	02-2003	Yu, Xianggang	341	118	
	AE1	6,577,261	06-2003	Brooks et al.	341	101	
	AF1	6,545,623	04-2003	Yu, Paul C.	715	513	
	AG1	6,466,153	10-2002	Yu, Paul C.			
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

PIP	AR	1	Kwan, "Shuffler Apparatus and Related Dynamic Element Matching Technique for Linearization of Unit-Element Digital to Analog Converters, Fig. 2a, US 2003/0137439				
PIP	AS	1	Yasuda et al., "A Third-Order Δ - Σ Modulator Using Second-Order Noise-Shaping Dynamic Element Matching," IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, pp. 1879-1886, IEEE (December 1998).				
PIP	AT	1	Kwan et al., "A Stereo Multibit $\Sigma\Delta$ DAC with Asynchronous Master-Clock Interface," IEEE Journal of Solid-State Circuits, Vol. 31, No. 12, pp. 1881-1887, IEEE (December 1996).				

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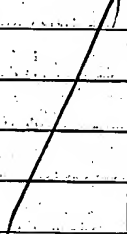
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2/24/04

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	AL2						Y s No
	AM2						Y s No
	AN2						Yes No
	AO2						Y s No
	AP2						Y s No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
PIP /	AR	2	Adams <i>et al.</i> , "A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, pp. 1871-1878, IEEE (December 1998).
PIP /	AS	2	Welz <i>et al.</i> , "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 48, No. 11, pp. 1014-1027, IEEE, (November 2001).
PIP /	AT	2	Grilo <i>et al.</i> , "A 12-mW ADC Delta-Sigma Modulator With 80 dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," IEEE Journal of Solid -State Circuits, Vol. 37, No. 3, pp. 271-278, IEEE (March 2002)

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	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
P/P	AR	3	Ian Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing Vol. 44, No. 10 pp. 808-817, IEEE (October 1997).
P/P	AS	3	Norsworthy <i>et al.</i> , Delta-Sigma Data Converters: Theory, Design and Simulation, pp. 185-186, IEEE Press, 1997.
P/P	AT	3	Zelniker <i>et al.</i> , Advanced Digital Signal Processing: Theory and Applications, pp. 357-364, Marcel Dekker, Inc. (1994).

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PIP	AR	4	Morteza Vadipour, "Techniques for Preventing Tonal Behavior of Data Weighted Averaging Algorithm in Σ - Δ Modulators," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 47, No. 11, pp. 1137-1144, IEEE (November 2000).
PIP	AS	4	Chen <i>et al.</i> , "Some Observations on Tone Behavior in Data Weighted Averaging," Proceedings of the 1998 International Symposium on Circuits and Systems, Vol. 1, pp. 500-503, IEEE (1998).
PIP	AT	4	Chen <i>et al.</i> , "An Improved Technique for Reducing Baseband Tones in Sigma-Delta Modulators Employing Data Weighted Averaging Algorithm Without Adding Dither," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 46., No. 1, pp. 63-68, IEEE (January 1999).

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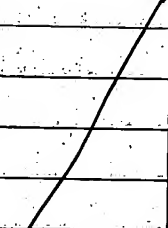
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OTHER (Including Author, Title, Date, Pertinent Pages, etc.)			
PUP	AR	5	Radke <i>et al.</i> , "A 14-Bit Current-Mode $\Sigma\Delta$ DAC Based Upon Rotated Data Weighted Averaging," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, pp. 1074-1084, IEEE (August 2000).
P4	AS	5	Baird <i>et al.</i> , "Improved $\Delta\Sigma$ DAC Linearity Using Data Weighted Averaging", pp. 13-16, IEEE (1995).
P/P	AT	5	Radke <i>et al.</i> , "A Spurious-Free Delta-Sigma DAC Using Rotated Data Weighted Averaging," IEEE 1999 Custom Integrated Circuits Conference, pp. 125-128, IEEE (1999).

EXAMINER <div style="text-align: center; font-family: cursive;">P. JEANPIERRE</div>	DATE CONSIDERED <div style="text-align: center; font-family: cursive;">5/24/04</div>
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	AM2						Y s
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	AN2						Yes
							No
	AO2						Yes
							No
	AP2						Yes
							No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

P/P	AR	6	Jensen et al., "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 45, No. 1, pp. 13-27, IEEE (January 1998)
P/P	AS	6	Annovazzi et al., "A Low-Power 98-dB Multibit Audio DAC in a Standard 3.3-V 0.35-μm CMOS Technology," IEEE Journal of Solid-State Circuits, Vol. 37, No. 7, pp. 825-834, IEEE (July 2002)
P/P	AT	6	Welz et al., "A Necessary and Sufficient Condition for Mismatch Shaping in Multi-Bit DACs," IEEE, pp. 1-105 to 1-108, IEEE (2002)

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	AM7					Yes
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	AN7					Yes
						No
	AO7					Yes
						No
	AP7					Yes
						No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

PIP	AR	Z	Fogleman et al., "A Digital Common-Mode Rejection Technique for Differential Analog-to-Digital Conversion," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 48, No. 3, pp. 255-271, IEEE (March 2002)
PIP	AS	Z	Lin et al., "A Bandpass Mismatch-Shaped Multi-Bit $\Sigma\Delta$ Switched-Capacitor DAC using Butterfly Shuffler," 1999 IEEE International Solid-State Circuits Conference, 0-7803-5129-0/99, IEEE (1999)
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